It is claimed that:

1. A riser comprising:

a plurality of riser codecs; and

an adaptive initialization module coupled to the riser codecs, the initialization module to configure the riser codecs when the riser is connected to a motherboard having a codec controller and a primary codec;

said initialization module to automatically select between a first multi-codec configuration and a second multi-codec configuration based on a codec support capability of the codec controller.

2. The riser of claim 1 wherein the first multi-codec configuration is a two-codec configuration and the second multi-codec configuration is a three-codec configuration.

3. The riser of claim 2 wherein the initialization module includes:

a detection module to monitor a status of a signal; and

an address controller coupled to the detection module and the riser codecs;

said address controller to select a two-codec address structure when the signal status indicates that the codec controller supports up to two codecs and a three-codec address structure when the signal status indicates that the codec controller supports up to three codecs.

4. The riser of claim 3 wherein the signal status indicates whether data is to be delivered from the primary codec to the codec controller in a two-codec configuration.

5. The riser of claim 3 wherein the three-codec address structure includes:

a first address corresponding to the primary codec;

a second address corresponding to a first riser codec; and

a third address corresponding to a second riser codec.

6. The riser of claim 3 wherein the initialization module further includes an enabling mechanism coupled to the primary codec, the enabling mechanism to disable the primary codec when the codec controller supports up to two codecs.

7. The riser of claim 6 wherein the two-codec address structure includes:

a first address corresponding to a first riser codec; and

a second address corresponding to a second riser codec.

8. The riser of claim 2 further including:

a printed wiring board electrically connecting the riser codecs to the initialization module; and

a connector coupled to the printed wiring board, the connector enabling electrical communication between the riser and the motherboard.

9. The riser of claim 8 wherein the connector has a data delivery pin, the data delivery pin enabling the initialization module to determine the codec support capability of the codec controller.

10. An adaptive initialization module, the initialization module comprising:

a detection module to monitor a status of a signal; and

an address controller coupled to the detection module;

said address controller to select a two-codec address structure when the signal status indicates that the codec controller supports up to two codecs and a three-codec address structure when the signal status indicates that the codec controller supports up to three codecs.

11. The initialization module of claim 10 wherein the signal status indicates whether data is to be delivered from a primary codec to the codec controller.

12. The initialization module of claim 10 wherein the three-codec address structure includes:

a first address corresponding to the primary codec;

a second address corresponding to a first riser codec; and

a third address corresponding to a second riser codec.

13. The initialization module of claim 10 further including an enabling mechanism coupled to the primary codec, the enabling mechanism to disable the primary codec when the codec controller supports up to two codecs.

14. The initialization module of claim 13 wherein the two-codec address structure includes:

a first address corresponding to a first riser codec; and

a second address corresponding to a second riser codec.

15. A riser comprising:

a plurality of riser codecs;

a detection module to monitor a status of a signal where the signal status indicates whether data is to be delivered from a primary codec to a codec controller;

an address controller coupled to the detection module and the riser codecs, said address controller to select a two-codec address structure when the control signal indicates that the codec controller supports up to two codecs and a three-codec address structure when the control signal indicates that the codec controller supports up to three codecs;

a printed wiring board electrically connecting the riser codecs to the detection module and address controller; and

a connector coupled to the printed wiring board, the connector enabling electrical communication between the riser and a motherboard.

16. The riser of claim 15 wherein the connector has a data delivery pin, the data delivery pin enabling the riser to determine a codec support capability of the codec controller.

17. A method of configuring a plurality of riser codecs, the method comprising:

monitoring a status of a signal where the signal status indicates whether data is to be delivered from a primary codec to a codec controller;

selecting a two-codec address structure when the signal status indicates that the codec controller supports up to two codecs; and

selecting a three-codec address structure when the signal status indicates that the codec controller supports up to three codecs.

18. The method of claim 17 further including determining whether a data delivery pin of a connector is terminated, the connector coupling a riser containing the riser codecs to a motherboard containing the primary codec and the codec controller.

19. The method of claim 17 further including:

placing the primary codec at a first address;

placing a first riser codec at a second address; and

placing a second riser codec at a third address.

20. The method of claim 17 further including:

disabling the primary codec;

placing a first riser codec at a first address; and

placing a second riser at a second address.

21. A computer-readable storage medium storing a set of instructions, the set of instructions capable of being executed by a processor to configure a plurality of riser codecs, the method comprising:

monitoring a status of a signal where the signal status indicates whether data is to be delivered from a primary codec to a codec controller;

selecting a two-codec address structure when the signal status indicates that the codec controller supports up to two codecs; and

selecting a three-codec address structure when the signal status indicates that the codec controller supports up to three codecs.

22. The computer-readable storage medium of claim 21 wherein the method further includes determining whether a data delivery pin of a connector is terminated, the connector coupling a riser containing the riser codecs to a motherboard containing the primary codec and the codec controller.